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| **Course Title** | **Digital Logic Design (Lab)** | | |
| **Course Code** | **CSC-315L** | | |
| **Credit Hours** | 1 (0,1) | | |
| **Category** | Computer Science Core | | |
| **Prerequisite** | None | | |
| **Co-Requisite** | None | | |
| **Follow Up** | CSC-215 Computer Organization & Architecture (Assembly language included) | | |
| **Course Introduction** | The course introduces the concept of digital logic, gates and the digital circuits. Further, it focuses on the design and analysis combinational and sequential circuits. It also serves to familiarize the student with the logic design of basic computer hardware components. | | |
| **Course Learning Outcomes (CLOs)** | At the end of the course, the students will be able to: | **BT** | **PLO** |
| | CLO1: Draw and interpret digital logic diagrams, including combinational and sequential circuits. | C2 (Understand) | 1,2,3 |
| | CLO 2: Design basic digital components such as multiplexers, flip-flops, and encoders. | C6 (Create) | 1 |
| | CLO 3: Analyze the behaviour of digital systems using truth tables and Boolean algebra. | C4 (Analyze) | 3 |
| | CLO 4: Implement simple digital circuits using logic gates. | C3 (Apply) | 1 |
| | CLO 5: Understand the fundamentals of digital system design and their applications. | C2 (Understand) | 1,2,8,10 |
| **Text Book(s)** | M. Morris Mano, Digital Logic and Computer Design, 1st Edition, Pearson, 1979, ISBN:0132145103. | | |
| **Reference Material** | 1. Thomas L. Floyd, Digital Fundamentals, 10th Edition, Prentice Hall, 2008, ISBN: 0132359235.<br>2. Fundamental of Digital Logic with Verilog Design, Stephen Brown, 2/e | | |

**Weekly Lesson Plan**

| Week No. | Course Content | Readings/Learning Activities |
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| **Week 1** | Familiarization with the Digital Electronic Trainer. | Mano: Chapter 1<br>Lab Tasks |
| **Week 2** | Implementation of logic gates using ICs,<br>AND Gate Operation<br>OR Gate Operation<br>Not Gate Operation | Mano: Chapter 2<br>Lab Tasks |
| **Week 3** | NAND Gate Operation<br>NOR Gate Operation<br>Conversion of NAND and NOR gates | Mano: Chapter 2<br>Lab Tasks |
| **Week 4** | Construction of XOR Gate from NAND&NOR Gate<br>Construction of XNOR Gate from NAND and NOR Gate<br>Construction of any circuit using NAND-only logic | Mano: Chapter 2<br>Lab Tasks |
| **Week 5** | Illustration of basic properties and theorems Boolean algebra using circuit design, | Mano: Chapter 2<br>Lab Tasks |

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| | Implementation of given Boolean functions | |
| **Week 6** | Using K-Maps for Function simplification and implementation | Mano: Chapter 3<br>Lab Tasks |
| **Week 7** | Half Adder,<br>Full Adder | Mano: Chapter 3<br>Lab Tasks |
| **Week 8** | Half Subtractor,<br>Full Subtractor | Mano: Chapter 3<br>Lab Tasks |
| **Week 9** | Design of 7-Segment Display | Mano: Chapter 4<br>Lab Tasks |
| **Week 10** | Decoder BCD To 7-Segment Display | Mano: Chapter 5<br>Lab Tasks |
| **Week 11** | Multiplexer,<br>Demultiplexer | Mano: Chapter 6<br>Lab Tasks |
| **Week 12** | Implementation of Boolean function(s) using Decoder and Multiplexer | Mano: Chapter 6<br>Lab Tasks |
| **Week 13** | Magnitude Comparator | Mano: Chapter 7<br>Lab Tasks |
| **Week 14** | D Latch and Flip-Flop Operation<br>Latching BCD Data for Displaying On 7- Segment Display | Mano: Chapter 7<br>Lab Tasks |
| **Week 15** | Shift Register Operation<br>JK Flip-Flop Operation | Mano: Chapter 7<br>Lab Tasks |
| **Week 16** | Random Access Memories | Mano: Chapter 4 – 6<br>Lab Tasks |